IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims:

1. (Currently Amended) A synchronicity detection apparatus for detecting a timing of a spread code having a cycle length T, which is included in a reception signal, comprising:

correlation coefficient generation means for dividing said spread code advancing a phase of said spread code every a certain first period, to generate a replica of said spread code;

a matched filter which performs detection of correlation values of said replica code generated by said correlation coefficient generation means and said reception signal every a certain second period;

a pseudo-random sequence generation means which generates a pseudo-random sequence from an initial value after supplying said pseudo-random sequence generated as said replica code;

wherein said matched filter has m levels of shift ~~registers~~register chips, T a larger value than the number of levels m,

wherein the replicas generated by the correlation coefficient generator change in sequence each time m chips are advanced, the replicas inputted to the matched filter are updated by a value whose phase advances by m chips each time a searchable range of m chips per certain first period advances;

~~wherein said certain first period is the time interval generated by m shift times;~~

wherein said synchronicity detection apparatus detects a local maximum correlation value over ~~a~~ the searchable range equal to said m shift registers; the searchable range being repeatcd plural times over the length T of the spread code.~~code;~~

~~a memory which cyclically adds said correlation values detected by said matched filter every said certain first period to store said added correlation values therein; and~~

~~means for detecting correlation energy from memory data in said memory means.~~

2. (Canceled)

3. (Previously Presented) The synchronicity detection apparatus according to claim 1, further comprising:

adding means which delays an output of the said matched filter by said certain first period to generate a delayed signal, and adds said delayed signal and thc said output of said matched filter, and

means for detecting a correlation value from the signal added by said adding means.

4. (Canceled)

5. (Original) The synchronicity detection apparatus according to claim 1, wherein said correlation coefficient generation means comprises:

a register which generates a certain pseudo-random sequence;

operation means which phase shifts a phase of said pseudo-random scquence generated by said register, and

means for supplying said phase-shifted pseudo-random sequence outputted by said operation means and said pseudo-random sequence outputted by said aforementioned register as said replica code.

6. (Previously Presented) The synchronicity detection apparatus according to claim 1, wherein said correlation coefficient generation means comprises replica code generation means for generating one unit of a second replica code from one unit of a first inputted replica code and generates one unit of a next replica code using one unit of said second replica code.

7. (Previously Presented) The synchronicity detection apparatus according to claim 1, wherein one unit of said spread code is each generated by repeating latch operations each time an operation clock of said correlation coefficient generation means is supplied predetermined number of times.

8. (New) A method for detecting a timing of a spread code having a cycle length T, which is included in a reception signal, comprising:

dividing the spread code advancing a phase of said spread code every a certain first period, to generate a replica of the spread code;

detecting with a matched filter correlation values of the replica code and the reception signal every a certain second period;

generating a pseudo-random sequence from an initial value after supplying the pseudo-random sequence generated as the replica code;

wherein the matched filter has m levels of shift register chips, T a larger value than the number of levels m,

wherein the replicas change in sequence each time m chips are advanced, the replicas inputted to the matched filter are updated by a value whose phase advances by m chips each time a searchable range of m chips per certain first period advances, and

detecting a local maximum correlation value over the searchable range, the searchable range being repeated plural times over the length T of the spread code.